IN THE SPECIFICATION

Please amend the Title on page 1, lines 1-2, as follows:

METHOD OF MANUFACTURING A NONVOLATILE SEMICONDUCTOR MEMORY DEVICE HAVING A STACKED GATE STRUCTURE ~~AND ITS MANUFACTURING METHOD~~

Please replace the paragraph at page 7, prenumbered lines 17-20, with the following rewritten paragraph:

Fig. 1 is a layout of a cell array of NAND type EEPROM according to Embodiment 1 of the invention. Figs. [[1A]] 2A and 2B are cross-sectional views taken along the A-A' line and B-B' line of Fig. 1.